

This Listing of Claims will replace all prior versions or listings of claims in this application.

LISTING OF CLAIMS

1. (Previously Presented) A communication device, comprising:
 - a signal modulator/demodulator (modem) having a digital signal processor for effecting radio communications;
 - an application processor (AP) having a central processing unit and a bus master controller for controlling via a first common bus a plurality of external peripherals ; and
 - a shared memory connected to the AP via the first common bus and connected to the modem via a second common bus,

wherein the bus master controller controls the plurality of external peripherals by using a packet generator issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals.
2. (Canceled)
3. (Previously Presented) The device of claim 1, wherein the shared memory is an SDRAM.

4. (Previously Presented) The device of claim 1, wherein the plurality of external peripherals include at least one of an image capture module, a display, and a flash memory.

5. (Canceled)

6. (Previously Presented) The device of claim 1, wherein the selected one of the plurality of external peripherals returns a signal to the bus master controller to acknowledge receipt of the packetized command.

7. (Previously Presented) The device of claim 1, wherein the packetized command packet includes:

a read/write command directed to shared memory shared by the modem and the AP.

8. (Previously Presented) The device of claim 7, wherein data read from the shared memory is sent to the AP with a strobe signal, and wherein the strobe signal is used for strobing the data read into a register in the bus master controller.

9. (Previously Presented) The device of claim 3, wherein the SDRAM includes a plurality of data banks and an interface for interfacing the bus master controller via the first common bus.

10. (Previously Presented) The device of claim 3, wherein the shared memory includes a first protection circuit for receiving address data from the AP and a second protection circuit for receiving address data from the modem, each for generating a protect signal upon simultaneously receiving the same address from the modem and the AP, wherein

the protect signal is generated to halt memory access by one of the modem and the AP in order to prevent simultaneous access of the same memory cells.

11. (Currently Amended) A communication device, comprising:

a signal modulator/demodulator (modem) having a digital signal processor for effecting radio communications;

an application processor (AP) having a central processing unit and a bus master controller for controlling via a first common bus connected to a plurality of external peripherals; and

a shared memory connected to the AP via the first common bus and connected to the modem via a second common bus,

wherein the bus master controller further controls a flash memory via the first common bus,

wherein the bus master controller controls the plurality of external peripherals operatively connected to the first common bus by issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals.

12. (Canceled)

13. (Previously Presented) The device of claim 11, wherein at least one peripheral of the plurality of external peripherals is an image capture module.

14. (Canceled)

15. (Currently Amended) The device of claim 14_11, wherein the selected one of the plurality of peripherals returns a signal over the first common bus to the bus master controller in the AP to acknowledge receipt of the packetized command.

16. (Currently Amended) The device of claim 14_11, wherein the packetized command includes:

a read/write command to the shared memory connected to the AP and the modem.

17. (Previously Presented) The device of claim 16, wherein data read from the shared memory is transmitted via the first common bus to the bus master controller in the AP with a strobe signal, and wherein the strobe signal is for strobing the data read into a register in the bus master controller.

18. (Previously Presented) The device of claim 11, wherein the shared memory is an SDRAM.

19. (Previously Presented) The device of claim 18, wherein the SDRAM includes a plurality of data banks and an interface for interfacing .

20. (Previously Presented) The device of claim 18, wherein the SDRAM includes a first protection circuit for receiving address data from the AP and a second protection circuit for receiving address data from the modem and for generating a protect signal upon simultaneously receiving the same address from the modem and the AP.

21. (Currently Amended) An application processor (AP), for use in a communication device, comprising:

a central processing unit for processing data received from a plurality of external peripherals; and

a bus master controller for controlling via a first common bus the plurality of external peripherals,

and for interfacing with a shared memory that is connected to a signal modulator/demodulator (modem) via a second common bus,

wherein the bus master controller controls the plurality of peripherals by issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packetized command includes a module device select signal used for selecting one of the plurality of external peripherals.

22. (Canceled)

23. (Previously Presented) The device of claim 21, wherein the shared memory is an SDRAM.

24. (Previously Presented) The device of claim 21, wherein the plurality of external peripherals additionally includes at least one of an image capture module, a display, and a flash memory.

25. (Canceled)

26. (Currently Amended) The device of claim 25_21, wherein the selected one of the plurality of external peripherals returns a signal to the bus master controller over the first common bus to acknowledge receipt of the packetized command.

27. (Currently Amended) The device of claim 25_21, wherein the packetized command includes:

a read/write command to the shared memory.

28. (Previously Presented) The device of claim 27, wherein the data read from the shared memory is sent over the first common bus to the AP with a strobe signal, and wherein the strobe signal is used for strobing the read data into a register of the bus master controller.

29. (Previously Presented) The device of claim 23, wherein the SDRAM includes a plurality of data banks and an interface for interfacing the bus master controller.

30. (Previously Presented) The device of claim 23, wherein the SDRAM includes a first protection circuit for receiving address data from the AP over the first common bus and a second protection circuit for receiving address data from the modem over the second common bus and for generating a protect signal upon simultaneous receipt of the same address from the AP and the modem.

31. (Currently Amended) An application processor (AP) for use in a communication device comprising:

a central processing unit for processing data received from a plurality of external peripherals over a first common bus; and

a bus master controller for controlling via the first common bus the plurality of external peripherals

and for interfacing with a shared memory that is connected to a signal modulator/demodulator (modem) via a second common bus,

wherein the bus master controller controls the plurality of external peripherals by issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals.

32. (Canceled)

33. (Previously Presented) The device of claim 31, wherein the shared memory is an SDRAM.

34. (Previously Presented) The device of claim 31, wherein the plurality of external peripherals include at least one of an image capture module, a display, and a flash memory.

35. (Canceled)

36. (Currently Amended) The device of claim 35 31, wherein the selected one of the peripherals returns a signal over the first common bus to the master controller to acknowledge receipt of the packetized command.

37. (Currently Amended) The device of claim 35 31, wherein the packetized command includes a read/write command directed to the shared memory shared by the modem and the AP.

38. (Currently Amended) The device of claim 37, wherein the data read from the shared memory is sent to the AP over the first common bus with a strobe signal, and wherein the strobe signal is used for strobing the data read into a register-register in the bus master controller.

39. (Previously Presented) The device of claim 33, wherein the SDRAM includes a plurality of data banks and an interface for interfacing with the bus master controller over the first common bus.

40. (Currently Amended) A method of controlling a communication device having a signal modulator/demodulator (modem) for effecting radio communications, an application processor (AP) having a central processing unit and a bus master controller, and a shared memory, the method comprising:

controlling via a first common bus a plurality of external peripherals using the bus master controller; and

interfacing with the modem via the shared memory and a second common bus,
wherein the step of controlling the plurality of external peripherals includes issuing a
packetized command commonly receivable by the plurality of external peripherals over the
first common bus, and

wherein the packetized command includes a module device select signal for selecting
one of the plurality of external peripherals.

41. (Canceled)

42. (Previously Presented) The method of claim 40, wherein the shared memory is
an SDRAM.

43. (Previously Presented) The method of claim 40, wherein the step of controlling
includes controlling at least one of an image capture module, a display, and a flash memory
included in the plurality of external peripherals.

44. (Canceled)

45. (Currently Amended) The method of claim-44~~40~~, wherein the selected one of
the plurality of external peripherals returns a signal to the bus master controller over the first
common bus to acknowledge receipt of the packetized command.

46. (Previously Presented) The method of claim 40, wherein the packetized
command includes a read/write command directed to the shared memory .

47. (Previously Presented) The method of claim 46, wherein data read from the shared memory is transmitted over the first common bus to the AP with a strobe signal, and wherein the strobe signal is for strobing the data read into a register in the bus master controller.

48. (Previously Presented) The method of claim 41, further including receiving address data from the AP over the first common bus and the modem over the second common bus at the shared memory and generating a protect signal upon simultaneously receiving the same address from the modem and the AP.

49. (Canceled)

50. (Canceled)